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Design and Implementation of 16-Bit Magnitude Comparator Using Efficient Low Power High Performance Full Adders

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ABSTRACT
In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder [1]. The paper attempts to examine the features of certain adder circuits which promise superior performance compared to existing circuits. The advantages of these circuits are low-power consumption, a high degree of regularity and simplicity. In this paper, the design of a 16-bit comparator is proposed. Magnitude comparison is one of the basic functions used for sorting in microprocessor, digital signal processing, so a high performance, effective magnitude comparator is required. The main objective of this paper is to provide new low power, area solution for Very Large Scale Integration (VLSI) designers using low power high performance efficient full adders.

Keywords: X greater than Y(XgY),X less than Y(XlY),X equal to Y(XeY) ,Power delay product (PDP),Low-Power(LP), High-Performance (HP), FA24T, N-10T,Bridge.

I. INTRODUCTION

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number. So comparator is used for this purpose. The comparator is a very basic and useful arithmetic component of digital systems that compares the magnitude of two binary numbers and determines if the numbers are equal, or if one number is greater than or less than the other number. One can implement the comparator by flattening the logic function directly Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes (Fig.1.1). The outcome of comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B

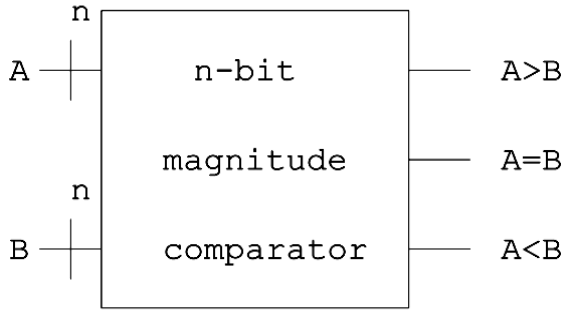


Figure 1.1: block diagram of n-bit magnitude comparator

The circuit, for comparing two n-Bit numbers, has 2n inputs & 2 2n entries in the truth table, for 1-Bit numbers, 2-inputs & 4-rows in the truth table, similarly, for 2-Bit numbers 4-inputs & 16-rows in the truth table. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance. A compact, good cost benefit, high-performance ratio comparator plays an important role in almost all hardware sorters

II. EFFICIENT FULL ADDER:

Some of the standard efficient full adders are compared and the full adder with less power is considered for the design of RCA and three stages of CSA.

2.1 REVIEW OF THREE STATE-OF-ART FULL ADDER CELLS

There are different types of CMOS full adder. This section reviewed the three state-of-the-art 1-bit full adders. This proposed cell is compared with them.

The Bridge circuit has 26 transistors this design creates a conditional conjunction between two circuit nodes. Full Adders which are based on fully symmetric CMOS style are called Bridge Full Adders.

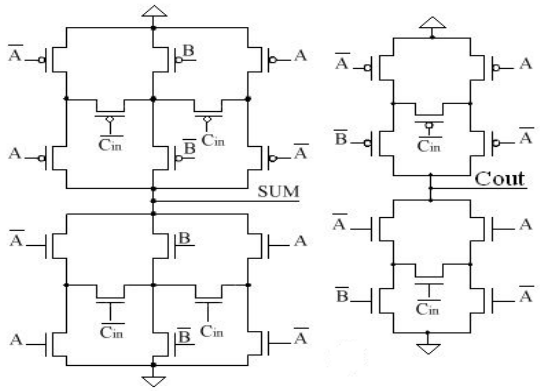


Figure 2.1: Bridge Full Adder

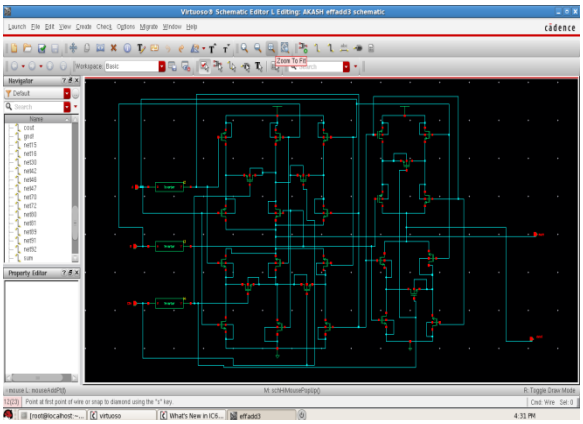


Figure 1.2: Schematic of bridge Full Adder

The full-adder with 24 transistors (FA24T) has 24 transistors this full Adder is based on Bridge style. The body of FA24T has two transistors less than Bridge and has better power consumption. In FA24t, a bridge circuit generates Cout and another bridge circuit is utilized in series with the prior to generate sum.

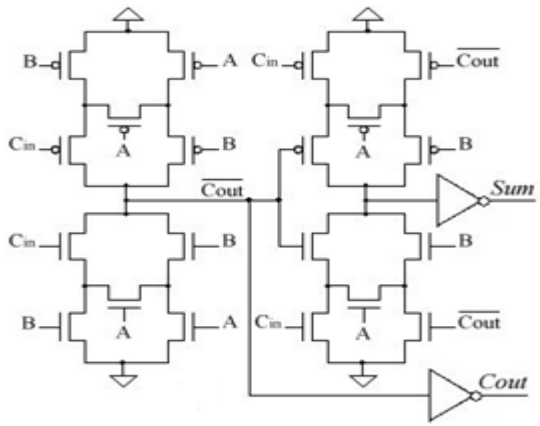


Figure 2.2: FA24T Full Adder

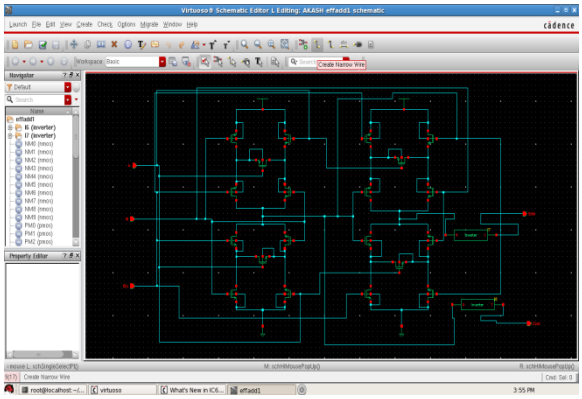


Figure 2.3: Schematic of FA24T Full Adder in cadence tool

The N10T full adder has only 10 transistors. Lowering the number of transistors is the advantage of this cell which leads to better performance and less silicon area. However poor driving capability and non full swing nodes are the serious problems of this full adder cell.

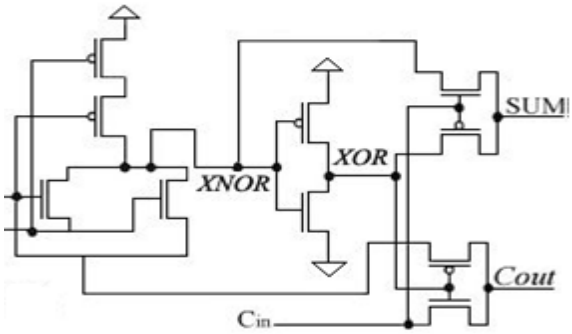


Figure 2.5: N-10T Full Adder

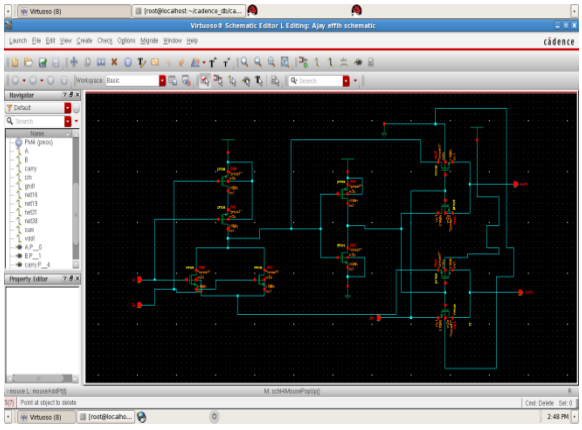


Figure 2.6: Schematics of N-10T Full Adder in Cadence tool

2.3 Layout of Efficient full-adder

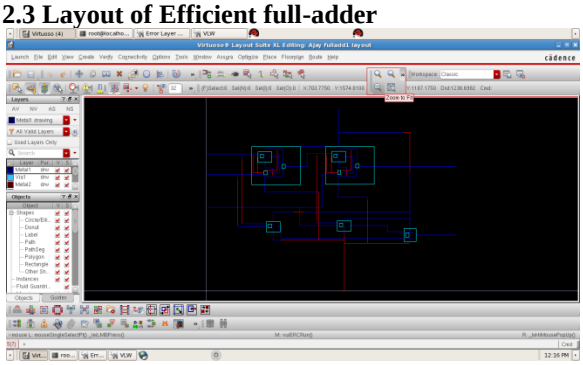


Figure 2.7: Layout of Efficient Full Adder

III. 1-BIT MAGNITUDE COMPARATOR

First of all we need to design an 1 bit comparator. We can easily make such a component, 2 bits for input A and B, and 2 bits for output X and Y. X is one when A is larger than B which means only when A is one and B is zero will set X to one. And for the Y, only when A and B both become one and zero will it be set. Here we can define.

X=AB’ Y=AB+A’B’

A	B	A>B	A=B
0	0	0	1
0	1	0	0
1	0	1	0
1	1	0	1

Table 3.1: OPERATION TABLE FOR 1-BIT COMPARATOR.

Second we draw the Karnaugh-map of 1-bit comparator and find the relationship between the input and the output. And en (enable input) is for cascading purpose.

X=AB’ (When A>B)

Y=AB+A’B’ (When A=B)

The circuit diagram of 1 bit comparator is shown in fig.2. Which is consist of Four two-input AND gates, One two-input NOR gate, Two inverters and one enable input.

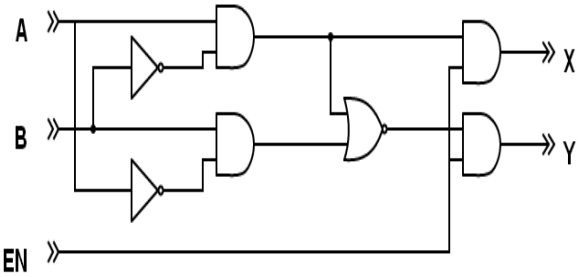


Figure 3.2: Schematic of conventional 1-bit comparator

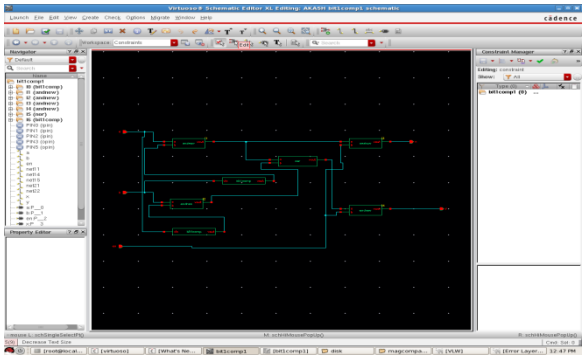


Figure 3.3: Schematic of conventional 1-bit comparator in Cadence tool

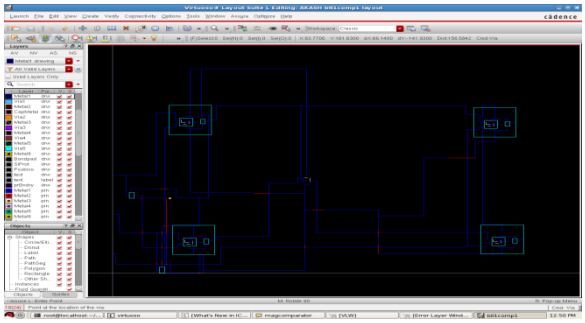


Figure 3.4: Layout of of conventional 1-bit comparator

IV. 16-BIT MAGNITUDE COMPARATOR USING EFFICIENT FULL ADDER

The implementation of 16-bit comparator is shown in figure below. To neither implement this we need 16 1-bit efficient Full Adders and one 16-input AND gate and a two input NOR gate. It has inputs (X16, Y16 X15,Y15 and so on up to X1,Y1).and for each Full Adder we have S and C as outputs. The output sum of each Full Adder(i.e S1 toS16) has been given to and gate the output of and gate determines whether XeY. Output carry C16 determines whether XgY The two outputs has been given to NOR gate and output of NOR gate determines whether XlY y is connected to enable input of each comparator and each x input is connected to 12-input OR gate.

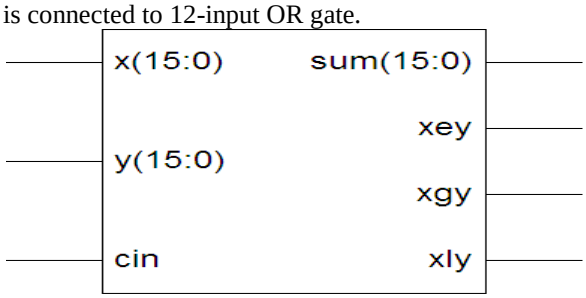


Figure 4.1: Schematic of conventional 16-bit comparator

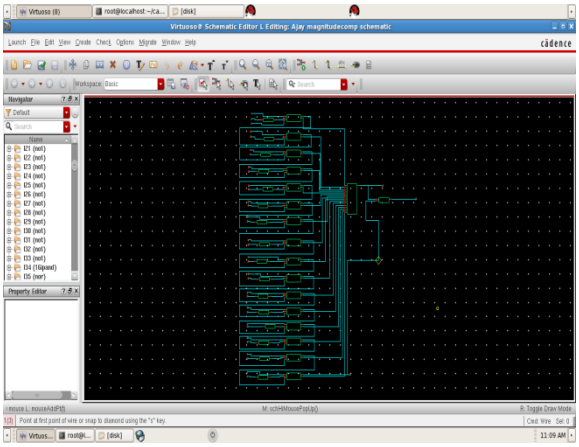


Figure 4.2: Schematic of 16-Bit Comparator using efficient Full Adder in Cadence tool ‘’

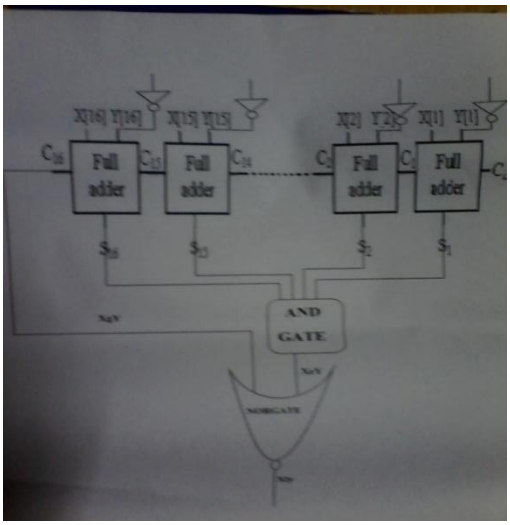
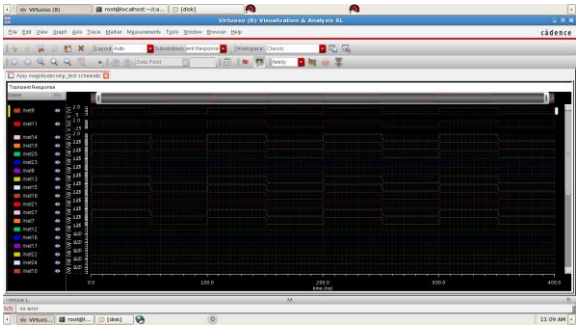


Figure 4.3: Schematic of 16-Bit Comparator using Efficient Full Adder

V. RESULT



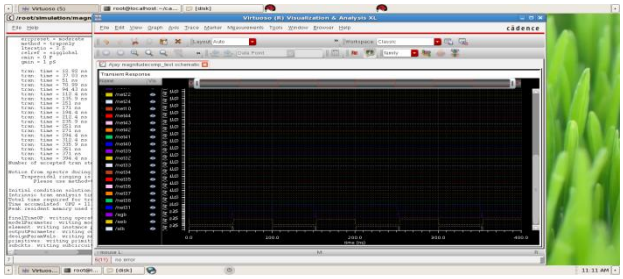


Figure 5.1: Simulation of 16-Bit Comparator in Cadence Tool

VI. COMPARATIVE ANALYSIS

Table 7.1: Comparison of Adders

Structure	No. of Transistors	Power (µw)	Delay (ns)	PDP
Bridge	26	1.66	104.2	172.97
FA24T	24	1.66	137.9	228.91
N-10T	10	1.13	73.5	83.05

Table 7.2: Parameters of Proposed 16-Bit efficient Comparator

Parameters	16-Bit Comparator using efficient Full Adder
Power(mW)	0.20
Delay(ns)	0.281
Speed(Msamples/sec)	3.55
Slices	22
LUT’s	38
IOB’s	52
Transistors	198

VII. CONCLUSION

Conventional 16-Bit comparator consume more power, more area and more delay. To overcome the problem of power, area and delay, the proposed design makes use of efficient full adders. Among the tested three efficient full-adders N-10T is found to be the most efficient full-adder. Therefore It has been found that the transistor count, power dissipation of the improved comparator using N-10T is less than that of the conventional comparator design .

VIII. ACKNOWLEDGEMENT

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